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Claims 1, 3, 16, and 18 have been amended.

The invention teaches a new method of filling gaps between a pattern of interconnect lines that forms a wiring structure on a semiconductor substrate. A network of interconnect lines has been created on a surface of a substrate whereby the interconnect lines are separated by spacings thereby leaving the surface of the substrate exposed between the interconnect lines. A first layer of dielectric is deposited over the interconnect lines including the exposed surface of the semiconductor substrate. An etch back of the first layer of dielectric is performed leaving the first layer of dielectric in place across the bottom of the spacings between the interconnect lines and partially over the top surface of the interconnect lines. A second layer of dielectric is deposited over the etched back first layer of dielectric. The second layer of dielectric is etched thereby creating exposed portions of the first layer of dielectric while leaving spacers containing the second dielectric on the upper portions of the sidewalls of the interconnect lines. A layer of oxide is deposited over the etched second layer of dielectric thereby including the exposed portions of the first layer of dielectric.

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Claim rejections - 35 U.S.C. § 112

Reconsideration of the rejection of claim 1, 3, 16, and 18 under U.S.C. § 112 is respectfully requested based on the following arguments.

Claims 1 and 16 have been amended to better clarify that the openings or holes that exist between the interconnect lines are filled with a dielectric material and in such a manner that keyholes do not occur between the interconnect lines.

In line 8-9 of claims 1,16, "said interconnect lies are separated by holes having bottoms between said interconnect lines", Examiner objects to this terminology as being unclear how the interconnect lines can be separated by holes because the interconnect line is a continuous mark to define a shape or contour whether a hole is a non-contiguous cavity or opening.

Applicant agrees with Examiner that an (one) interconnect line is a continuous mark to define a shape or contour, the terminology as used by Applicant refers to a plurality of interconnect lines, this plurality of interconnect lines infers that each of the interconnect lines has adjacent interconnect

lines, between a given interconnect line and the interconnect lines that are adjacent to this interconnect line there are, according to the terminology that is used by Applicant, spacings of holes that separate the interconnect lines so as to avoid one solid mass of metal in which case the interconnect lines would no longer be interconnect lines but would revert back to the original state of the layer of metal that has been used to create (pattern and etch)OP the interconnect lines. One interconnect line cannot be separated by holes, a plurality of interconnect lines can and must be separated by holes so that the interconnect lines can indeed function as interconnect lines.

In line 9-11 of claim 1, "leaving said surface of said substrate partially exposed over said bottoms of said holes between said interconnect lines". Examiner objects to this terminology as being vague and indefinite and interprets the word "hole" as meaning a cavity or opening in the solid. If therefore, according to Examiner's interpretation, "the substrate is exposed over the bottoms of said hole" then this cavity is, according to Examiner's interpretation, filled and it is not a hole anymore.

Regarding claims 17-20, 22-23, 24, 26, the limitations that are advanced by Examiner relating to these claims have been discussed above.

Claim 1, lines 7 states that a network of interconnect lines is created on the surface of a substrate, the creation can only be accomplished by first depositing a layer of metal after which the layer of metal is patterned and etched. The etching partially removes the patterned metal, where the metal is removed during and as a result of the etching process, the surface of the underlying substrate is exposed (since this surface is no longer covered with the metal the is patterned and removed). Not all of the metal however is removed from the surface of the substrate, the interconnect lines are formed by leaving a pattern of metal in tact on the surface of the substrate. In sum: the interconnect lines form a pattern of metal that remains deposited on the surface of the substrate, where the metal is removed from the surface of the substrate openings (or holes) are created in the original (prior to patterning and etching) layer of metal. By nature of the fact that the metal is partially removed from the surface of the substrate, this surface becomes partially exposed. The exposure of the substrate occurs where the original metal is removed, that is between the metal that remains in place, which is

between the pattern of interconnecting lines. No cavity is therefore filled, the opposite occurs by creating cavities (referred to as holes by Applicant), these holes have bottom which is the exposed surface of the underlying substrate (that is the surface on which the pattern of interconnect lines is formed).

Rejection of claims 1-5, 8-12, 14-15 under 35 U.S.C. 103(a).

1. Reconsideration of rejection of claims 1-5, 8-12, 14-15 under 35 U.S.C. 103(a) as being unpatentable over Parat et al. (US 5,731,242) in view of Lee (US 5,663,092) under 35 U.S.C. § 103 is respectfully requested based on the following arguments.

Parat et al. (US 5,731,242) teach a method for forming closely spaced gate structures while avoiding shorts between gate contacts and the gate structures, the Parat et al. (US 5,731,242) method therefore allows for increased density of gate stacks.

The Parat et al. (US 5,731,242) method starts with a gate structure that may contain several conductive layers formed over a layer of gate oxide that has been created on the surface of a

substrate. The gate structure has the conventional regions of different conductivity (well regions, source/drain regions) while the gate structure contains a lower layer that functions as a floating gate and an upper layer that functions as a word line or control gate for a flash EPROM cell.

The present invention limits itself to a process that addresses interconnect lines that are created on the surface of a substrate, no additional layers or impurity implants are performed as part of the process of the present invention.

Parat et al. (US 5,731,242) continues with the formation of an insulative layer (of for instance SiO2, for improved charge retention capabilities of floating gate of the EPROM cell) over which a etch stop layer (of for instance SiN, to protect each gate structure during contact etching and to further insulate each gate structure from the contact filling) is deposited. These latter two layers remain deposited on the surface of the gate structures after the gate structures have been etched from the conductive layers.

The present invention does not apply either a layer of insulation or a layer of etch stop material since the objectives of the present invention fundamentally differ from the

objectives of the method that is provided by Parat et al. (US 5,731,242). The instant invention deposits a layer of dielectric over the pattern of interconnect lines including the surface of the substrate that is exposed between the interconnect lines. Parat et al. (US 5,731,242) grow a layer of oxide on the sidewalls of the gate stack for insulation of the gate stack (from the contact etching). The instant invention deposits a first layer of dielectric over the interconnect lines including the surface of these lines. The first layer of dielectric of the present invention is etched and leaves a pattern and profile of dielectric in place that materially assists in avoiding key-holes and other irregularities of deposition (non-uniform dielectric density distribution) of the layer of dielectric that is, under the present invention, deposited over the first (etched) layer of dielectric.

Parat et al. (US 5,731,242) deposit a layer of silicon nitride over the upper surface of the gate structure (the patterned etch stop layer) and over the surface of the first layer of dielectric. This to further enhance the objective of the Parat et al. (US 5,731,242) invention, that is to create improved isolation between the gate electrode and the gate contacts. This layer of silicon nitride is etched whereby the silicon nitride is removed from the bottom of the openings

between the gate electrodes so that electrical contact can be established with the source/drain regions of the gate electrodes. The present invention deposits a second layer of dielectric over the etched first layer of dielectric and, due to the specific profile of the surface of the first layer of dielectric (first dielectric remaining on the bottom of the openings between the interconnect lines and on the upper surface of the interconnect lines), deposits the second layer of dielectric immediately adjacent to the exposed sidewalls of the interconnect lines, thereby allowing the second layer of dielectric to be etched and forming pronounced spacers on the sidewalls of the interconnect lines. The objective of the Parat et al. (US 5,731,242) etch of the second layer of dielectric is to create contact openings to the gate structures, the etch of the layer of silicon nitride under Parat et al. (US 5,731,242) removes all of the silicon nitride from the top of each stack and from the silicon substrate; none or only an insignificant amount of silicon nitride is removed from the side of each stack while the nitride sidewalls will not typically extend al the way down to the underlying substrate (Column 6, lines 30-39). The sidewalls that are therefore formed under Parat et al. (US 5,731,242) are significantly different from the second layer of dielectric that remains in place under the present invention.

Parat et al. (US 5,731,242) completes the process of the invention with completing contacts to the gate structures, thus forming closely spaced EPROM cells. The present invention deposits a layer of PE-TEOS or PE-oxide over the two etched layers of dielectric and, due to the specific profile that the surface of the two etched layers of dielectric presents, the deposit layer of PE-TEOS or PE-oxide has a uniform density distribution and avoids the formation of voids or other undesirable irregularities within the deposited layer of PE-TEOS or PE-oxide.

Parat et al. (US 5,731,242) does not perform an etch-back of the first layer of dielectric because such an etch-back would defeat the purpose of the Parat et al. (US 5,731,242) method, that is to allow for closer spacing between EPROM cells. Parat et al. (US 5,731,242) perform an etch-back of the second layer of dielectric whereby however this etch-back is required to form contact openings to the source/drain regions of the gate stack. This second etch-back further uniformly removes the second dielectric from the upper surface of the gate stacks while, as previously stated, only an insignificant amount of the second dielectric is removed from the side of each stack while the nitride sidewalls will not typically extend al the way down to the underlying substrate.

Lee (US 5,663,092) discloses the step of etching back dielectric layer from the upper surface of a wiring structure, this etch-back is performed (Fig. 8) in order to create a channel line contact for contacting a first of the source/drain regions of gate electrodes (column 5, lines 42-43). This etch-back therefore is a partial removal of the dielectric from the upper surface of the gate electrode and does not require any special considerations that are imposed by an underlying first layer of dielectric. Nor is there an underlying layer of first dielectric present (Fig. 7), the layer of dielectric that is partially removed overlies a capped gate line.

Regarding claims 2-4, Parat et al. (US 5,731,242) discloses the formation of gate structures that address design requirements of an EPROM cell with floating gates, control gates and the like. The present invention is not limited to any specific, gate electrode or EPROM cell design imposed limitations that restrict the use of the material that is used for the interconnect lines. Polysilicon is therefore specified as a specific material (claims 2 and 3) while the invention can be applied using any electrically conductive material (claim 4). The self-aligned contact process that is used by Parat et al. (US 5,731,242) is used for the (typical) self-aligned impurity

implants for source/drain regions adjacent to the gate structures.

Regarding claim 5, while the use of high density plasma is well known in the art, it has experimentally been found the this material is best suited and provides optimum results under the process of the invention. High Density Plasma oxide ahs therefore been claimed as the preferred material to be used for the first layer of dielectric.

Regarding claim 9, it has again been experimentally determined that Si_3N_4 is the optimum material for the process of the invention for the second layer of dielectric while the optimum method that can be used for the deposition of the second layer of dielectric is the method of PECVD. It must be remembered that the method of the invention depends significantly on the success that is obtained in shaping and controlling the profile of the surface of the first and the therewith combined second layer of dielectric. The layer of silicon nitride that is deposited under Parat et al. (US 5,731,242) (layer 280, Fig. 8) is uniformly deposited over the underlying surfaces and serves as an etch stop layer.

Regarding claim 10, the layer of second layer of dielectric although it can contain, in accordance and as previously claimed under Parat et al. (US 5,731,242), a layer of aluminum oxide, the second layer of dielectric is under the present invention deposited over the first layer of dielectric that remains in place over the bottom of the openings between the pattern of interconnecting lines whereby the profile of the surface of the first layer of dielectric and with that the profile of the surface of the deposited second layer of dielectric are patent objective dependent and vary significantly from profiles and objectives that are in force under Parat et al. (US 5,731,242). The layer that may contain aluminum oxide under Parat et al. (US 5,731,242) is an etch stop layer (layer 238, Fig. 8) that is essentially uniformly deposited over the surface of a gate stack. The second layer of dielectric of the invention, while containing aluminum oxide, is deposited over the previously etched and specifically profiled, first layer of dielectric nad therefore serves a purpose and has a deposition profile that is significantly different from the layer of aluminum oxide that is used under Parat et al. (US 5,731,242). Parat et al. (US 5,731,242) is silent on whether the second layer of dielectric covers the partially exposed surface of interconnect lines for the reason that under Parat et al. (US 5,731,242) there are no partially exposed surfaces of interconnect lines since such a

partial exposure would completely negate the objective of the Parat et al. (US 5,731,242) invention, that is to be able to reduce the distance between adjacent EPROM cell. Exposure of interconnect line (gate structures) would result in shorts between the gate stacks and the contact to the gate stacks making the gate stacks not functional. For the Lee disclosure, the second and third dielectric layers are sued for gate spacer formation and for top surface isolation of the gate stacks. These layers are therefore uniformly deposited and/or etched and are shaped to a thickness that meets the objectives that are imposed on these layers. For top surface gate isolation, the layer is uniformly shaped, for gate spacers the conventional profile is followed whereby the spacers adhere to the sidewalls of the gate stacks and all along the sidewalls of the gate electrode.

Regarding claim 12, It is key to the present invention that the second dielectric is etched in a particular manner, the is leaving the second dielectric in place above the previously etched and profiled first layer of dielectric and forming spacers on the sidewalls of the interconnect lines. The difference between Parat et al. (US 5,731,242) and the present invention is basic in that Parat et al. (US 5,731,242) etches to form conventional gate spacers while the present invention

etches the second layer of dielectric to form a yet more contoured layer of dielectric, comprising the etched first and second layers of dielectric, that forms the base on which the final layer of PE-TEOS or PE-oxide is deposited. The requirement as specified in claim 12 is therefore basic to the present invention while the etch of Parat et al. (US 5,731,242) differs significantly from the etch of the invention.

Regarding claim 14, while the use of PE-oxide or PE-TEOS is well known in the art, the use of these materials as part of the completion process of the invention has been experimentally confirmed as providing the optimum results of creating a stress free and uniform layer of dielectric. The layer of PE-oxide or PE-TEOS, in combination with the specified layer of SiN that is used for the spacers on the sidewalls of the interconnect lines and the layer of HDP oxide that is used for the first layer of dielectric and that partially remains in place between the interconnect lines, forms an optimum intra-level dielectric (ILD) also from the point of view of having a low dielectric constant for this layer of ILD.

Regarding claim 15, the process of planarizing deposited layers of semiconductor materials is well known in the art. This claim is included as part of the process of the invention in

view of the fact that the process of the invention creates a uniform layer of dielectric overlying the interconnect pattern and that therefore the process of planarization of this dielectric can be performed without causing surface irregularities in the planarized surface. In the absence of the process of the invention, the step of planarizing may lead to surface irregularities that may have a negative impact on device performance (intra-conductive line leakage) or device creation (lack of surface planarity with the consequent negative impact on steps of photolithography that may be applied to create overlying layers).

In light of the foregoing arguments, applicant respectfully requests that the Examiner's rejection of claims 1-5, 8-12, 14-15 under 35 U.S.C. 103(a) as being unpatentable over Parat et al. (US 5,731,242) in view of Lee (US 5,663,092) under 35 U.S.C. § 103 be withdrawn.

2. Reconsideration of rejection of claims 6-7, 16-24, 26 under 35 U.S.C. 103(a) as being unpatentable over Parat in view of Lee and further in view of Jeng et al. (US 5,683,922) is respectfully requested base on the following arguments.

Regarding claim 6 and 7, whereby Parat and Lee are silent about the used of buffered oxide etch for the etching of the first layer of dielectric, a further examination of the profile of the surface of the first layer of dielectric after this layer has been etched (Fig. 5 of the instant invention) shows that this profile is unique and forms a dependency for the successful application of the process of the invention. A layer of first dielectric remains in place over the bottom of the opening that exists between adjacent interconnect lines, in addition a peak shaped amount of first dielectric remains in place on the upper surface of the interconnect lines. Both of these remaining deposits are required since both remnants are instrumental in the preparation for the final step of the processes of the invention. The etched first layer of dielectric forms the basis on which the second layer of dielectric of the invention is deposited after which the second layer of dielectric is etched. If the etched first layer of dielectric does not have the required profile, the second layer of dielectric cannot be properly deposited resulting in undesirable results of the overall process. It is therefore important that the profile of the surface of the etched first layer of dielectric meets requirements of support for the deposition of the second layer of dielectric. For this reason the etching of the first layer of dielectric must be precisely controlled which is the reason that

this process of etch is specified in claims 6 and 7. Claims 7 and 21 in view of the above argument specify etch conditions for the etch-back of the first layer of dielectric. Etchant ratios can be varied in accordance with specific desired characteristics of the etch that is performed, it is however claimed that the etch conditions that have been specified as part of the present invention best meet the objectives of this invention and are therefore of importance to the invention.

In light of the foregoing arguments, applicant respectfully requests that the Examiner's rejection of claims 6-7, 16-24, 26 under 35 U.S.C. 103(a) as being unpatentable over Parat in view of Lee and further in view of Jeng et al. (US 5,683,922) be withdrawn.

3. Reconsideration of rejection of claims 13 under 35 U.S.C. 103(a) as being unpatentable over Parat in view of Lee as applied to claim 1 and further in view of Kasai (US 5,821,594) is respectfully requested base on the following arguments.

Kasai (US 5,821,594) provides for a method of forming an insulated gate field effect transistor having a self-aligned type contact hole. Kasai (US 5,821,594) as part of the processing sequence that is used for the formation of the stated

device, applies layer of semiconductor material and processes these layers. As part of this process, special attention is being paid to the formation of the contact hole with the creation of a sub-micron MOS transistor. The essential description of the Kasai (US 5,821,594) invention focuses on the creation of a single MOS transistor and the steps that are required to form contact to this transistor. For these processes, Kasai (US 5,821,594) using a sequence of material depositions that include the deposition of a gate insulation layer, a protective insulation layer formed on the upper surface and the sidewalls of the gate electrode and the like. As part of this process, Kasai (US 5,821,594) does not address the formation of stress-free layers of dielectric for either Inter Level Dielectric or Intra-Metal Dielectric. Also, Kasai (US 5,821,594) does not indicate specific methods and conditions of etching of a layer of dielectric, such as is specified in Claim 13 of the present invention. The method of the present invention does specify the processing conditions for the etching of the second layer of dielectric (claim 13) since this etch is also critical to the successful application of the process of the invention. The profile of the surface of the second layer of dielectric, combined with the profile of the surface of the first layer of dielectric form the basis over which the final layer of dielectric is deposited. This profile must therefore be

precisely shaped which in turn required that the conditions that affect this shaping must be well understood. These conditions have been specified in Claim 13.

In light of the foregoing arguments, applicant respectfully requests that the Examiner's rejection of claim 13 under 35 U.S.C. 103(a) as being unpatentable over Parat in view of Lee as applied to claim 1 and further in view of Kasai (US 5,821,594)) be withdrawn.

4. Reconsideration of rejection of claims 25 under 35 U.S.C. 103(a) as being unpatentable over Parat, Lee and Jeng as applied to claim 16 and further in view of Kasai (US 5,821,594) is respectfully requested base on the following arguments.

The method of the present invention specifies the processing conditions for the etching of the second layer of dielectric (claims 13, 25) since this etch is critical to the successful application of the process of the invention. The profile of the surface of the second layer of dielectric, combined with the profile of the surface of the first layer of dielectric form the basis over which the final layer of dielectric is deposited. This profile must therefore be precisely shaped which in turn required that the conditions that

affect this shaping must be well understood. These conditions have been specified in Claim 13 and claim 25. It is clear that experimentation can be performed that has as objective to determine the optimum conditions that apply to the processes of etching the first and the second layers of dielectric under the processing sequence of the invention. This experimentation has in fact been performed and has resulted in the [processing conditions that are specified in claims 13 and 25. Without these specific processing conditions, the process of the present invention is not complete which is the very reason that these conditions are included as part of the specification of the invention. It is not enough to indicate that certain depositions and configurations theoretically can be realized, to give the process of the invention as firm basis of reality the processing conditions that are required to realize the suggested depositions of the dielectrics are included thereby connecting the method of the invention with actual conditions and the actual realization of the process of the invention.

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In light of the foregoing arguments, applicant respectfully requests that the Examiner's rejection of claim 25 under 35 U.S.C. 103(a) as being unpatentable over Parat, Lee and Jeng as applied to claim 16 and further in view of Kasai (US 5,821,594) be withdrawn.

5. The prior art made of record and not relied upon that is considered pertinent to Applicant's disclosure, that is Chen et al. (US 5,858,869) disclosing the deposition of dielectric silicon oxide using plasma enhanced; Liaw (US 5,807,779) disclosing the deposition of silicon nitride using PECVD have been examined and have been found to be of general interest to the invention. These prior art records however do not teach the extent and the detail combined with the flexibility of the present patent application.

While applicant acknowledges the teachings of Parat et al. (US 5,731,242), Lee (US 5,663,092), Liaw (US 5,807,779), Chen et al. (US 5,858,869) and Jeng (US 5,683,922) as cited by the Examiner, and although applicant does not necessarily agree that the Examiner's arguments show sufficient and proper basis for suggestion or motivation to modify or combine Parat et al. (US 5,731,242) and Lee (US 5,663,092), Parat et al. (US 5,731,242) and Liaw (US 5,807,779), Parat et al. (US 5,731,242) and Jeng

(US 5,683,922), Parat et al. (US 5,731,242) and Chen et al. (US 5,858,869) applicant nonetheless also asserts that there is absent within the portions of Parat et al. (US 5,731,242), Lee (US 5,663,092), Liaw (US 5,807,779), Chen et al. (US 5,858,869) and Jeng (US 5,683,922) or any combination thereof, as cited by the Examiner, an express or inherent teaching of each and every limitation within applicant's invention as taught and claimed within claims 1-26.

In this regard, applicant claims that there is absent form the portions of Parat et al. (US 5,731,242), Lee (US 5,663,092), Liaw (US 5,807,779), Chen et al. (US 5,858,869) and Jeng (US 5,683,922) or any combination thereof, as cited by Examiner, a teaching of creating a specific profile by successively etching two layers of dielectric such that a layer of dielectric that is deposited over the surface of the two etched layers of dielectric can be deposited free of internal stress and with a uniform density throughout the deposited layer of dielectric.

None of the applied or known references address the invention as shown in the amended claims in which a uniform layer of dielectric can be deposited over the surface of a layer of interconnect lines. The invention is believed to be patentable over the prior art cited, as it is respectfully

suggested that the combination of these various references cannot be made without reference to Applicant's own invention. None of the applied references address the problem of internal irregularities of a deposited layer of dielectric. Applicant has claimed his process in detail. The processes of Figs. 3 through 8 are both believed to be novel and patentable over these various references, because there is not sufficient basis for concluding that the combination of claimed elements would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination. We therefore request Examiner B. Tran to reconsider his rejection in view of these arguments and the amendments to the Claims.

Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

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SUMMARY

Applicant's invention as claimed is directed towards a novel method of forming a layer of dielectric overlying a pattern of interconnect lines. A first layer of dielectric is deposited over the interconnect lines including the exposed surface of the semiconductor substrate. An etch back of the first layer of dielectric is performed leaving the first layer of dielectric in place across the bottom of the spacings between the interconnect lines and partially over the top surface of the interconnect lines. A second layer of dielectric is deposited over the etched back first layer of dielectric. The second layer of dielectric is etched thereby creating exposed portions of the first layer of dielectric while leaving spacers containing the second dielectric on the upper portions of the sidewalls of the interconnect lines. A layer of oxide is deposited over the etched second layer of dielectric thereby including the exposed portions of the first layer of dielectric.

It is requested that should Examiner not find the claims to be allowable that he call the undersigned Attorney at his convenience at 914-452-5863 to overcome any problems preventing allowance.

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Respectfully submitted,

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